When to use an off-the-shelf PCI Express device versus an FPGA

By Krishna Mallampati

Deciding when to design a circuit or use an off-the-shelf solution is a challenge board designers face everyday. Sometimes it makes sense to implement off-the-shelf PCI Express devices, while other times, developing application-specific solutions using FPGAs seems to be a better option. Krishna examines what criteria should be weighed in making this decision.

FPGAs are possibly the most ubiquitous semiconductor devices in the industry. It’s a rare engineer who hasn’t used these devices at some point in his or her career, whether as a student or professionally in hardware/software design. In the past 20 years, FPGAs have evolved to support an ever-increasing range of functions for virtually every market segment: telecommunications, test and measurement, industrial, military and aerospace, automotive, medical, storage, servers, and consumer electronics. With Altera and Xilinx commanding 85 percent of the programmable logic market, designers don’t have countless choices; it’s as simple as deciding between Pepsi and Coke!

FPGAs are mandatory in applications where:

- Reprogrammability in the field is essential
- A design is not complete but vendors need proof of concept

A significant amount of proprietary IP differentiates a vendor’s product in the market

Volumes are low and time to market is of the essence

On the other hand, FPGA usage doesn’t make sense in some applications. If an Application-Specific Standard Product (ASSP) can implement the exact same function a designer needs at a fraction of the cost of FPGAs without the hassle of pulling together several components, is available in production volumes, and is shipping to several hundreds of designers, then FPGAs aren’t the right option.

In one such application the design calls for a PCI Express (PCIe)-to-generic local bus bridge device. Designers in this instance have two very distinct choices:

1. Use an FPGA, configuration device, external PHY, PCIe IP, and design software, then integrate all of them and verify the function
2. Simply use a single-chip solution in the form of a PCIe-to-local bus bridge device

Examples of the first scenario include Altera’s Cyclone II FPGA + TTI’s PHY and Xilinx’s Spartan-3/E FPGA + Philips PHY; of the second scenario, PLX’s PEX 8311 local bus-to-PCIe bridge.

By choosing a single-chip solution for this function, designers can realize several advantages, such as:

- Lower overall cost
- Minimal board space
- Less engineering resources to integrate and verify multiple devices
- Increased performance and features
- Fewer support issues
- Less devices in inventory

Even in a design where an FPGA already exists, designers can easily implement PCIe with the PCIe-to-local bus bridge instead.
of using an external PHY, PCIe IP, then integrating these into the FPGA and verifying the operation. Designers then not only save the cost of an external PHY and PCIe IP but also do not need bigger, more expensive FPGAs and configuration devices to fit the PCIe IP in addition to their proprietary IP.

The local bus is a generic bus with 32 bits of data and a 33 MHz/66 MHz clock that has been around for more than a decade. Thousands of embedded applications out there have a local bus integrated into a design. With PCIe becoming a mainstream serial interface, offering higher bandwidths with fewer pins and lower prices due to the high volumes being used, designers using a local bus would realize tremendous benefits by migrating their designs to PCIe.

Some real-world applications highlight how a PCIe-to-local bus bridge device can be used instead of FPGAs and coexist with FPGAs.

**Industrial control video monitor**

Because FPGAs are memory-intensive devices, designers can use FPGAs for acquiring, storing, and processing images in a video monitoring system such as those used in surveillance, security, industrial, or business applications (see Figure 1). However, transmitting several of these high-resolution images to a central station where guards are monitoring the location would require a high-speed interface such as PCIe. The PEX 8311, for example, would connect to the FPGAs on the local bus and transmit these images to a central command station over PCIe. A PCIe switch such as the PEX 8508 then would acquire images from several of the bridge devices and display them in a central location.

**System controller card**

In a controller card application (Figure 2), a bridge device in addition to bridging local bus to a PCIe interface must also support a large number of devices on the local bus. A bridge can support up to six devices on the local bus and provide a PCIe interface to all these devices.

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**Table 1**

<table>
<thead>
<tr>
<th>Feature</th>
<th>PLX Single chip</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complete local bus to PCIe bridge</td>
<td>Yes</td>
<td>Only PCIe core</td>
</tr>
<tr>
<td>Cost of PCIe IP</td>
<td>Included</td>
<td>x1 lane = $15K</td>
</tr>
<tr>
<td>Chip count</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>PHY cost</td>
<td>Included</td>
<td>Additional</td>
</tr>
<tr>
<td>Mandatory configuration device</td>
<td>Not needed</td>
<td>Additional</td>
</tr>
<tr>
<td>Software</td>
<td>Included</td>
<td>Quartus II v5.1 (Altera) ISE 8.1i (Xilinx) Additional license fee for either</td>
</tr>
<tr>
<td>Support for six loads on local bus at 66 MHz</td>
<td>Yes</td>
<td>No</td>
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