The state of RapidIO: strong, proud, and open

By Tom Cox

The RapidIO technology is quickly gaining traction as a leading parallel and serial interconnect with plenty of activity in the specification and in the markets. Tom Cox, executive director of the RapidIO Trade Association, shares his views of the state of RapidIO.

The RapidIO Trade Association, like many industry standards organizations, was formed to develop a specification and promote the common business interest of its members. These members are only one of the keys to the tremendous success of this international industry standard. They are the providers of the networking, telecom, storage, signal processor, and high-performance embedded applications industries. Members, with a common interest alone do not make a successful association or ensure that the other necessary elements are in place to:

- Create a viable and strong ecosystem
- Support the creation of interoperable, scalable, and reliable I/O products
- Develop international open industry standards for a high-performance, packet-switched, system-level interconnect with a viable, long-term road map

RapidIO technology is based on a truly open, established switched fabric standard designed by embedded engineers to power applications in military, industrial, wireless, triple play, multimedia, and other communications markets, and to deliver the reliability, cost effectiveness, performance, and scalability required by OEMs building next-generation equipment today. The RapidIO Trade Association is governed by industry leaders AMCC, EMC, Ericsson, Freescale Semiconductor, Lucent Technologies, Mercury Computer Systems, PMC-Sierra, Texas Instruments, Tundra Semiconductor, and Wind River.

The embedded marketplace is constantly moving and evolving, and designers are bombarded endlessly with new technologies and products, all claiming to provide the most compelling solution.

These new and improved solutions leave many questions to be answered. Can the technology do the job? What’s the long-term road map? Can I get all the components I need to build the system? Will the components work together seamlessly? Are parts available from my current suppliers? Are other competitors using this technology? Can I develop a cost/performance advantage with this solution?

The RapidIO Trade Association has developed a world-class technology, the largest, strongest embedded ecosystem of suppliers, proven interoperability, a broad range of interworking abilities with PCI, PCI Express, and message passing (for example, Ethernet encapsulation). All these come with a road map that adds functionality and technology to keep pace with systems’ cost and performance demands.

Ecosystem

A strong and growing ecosystem is the first critical proof point designers need to see before they even consider a new technology. Too often embedded designers look only to ecosystems that were established to support the PC industry. In the early days of embedded design, that may have been sufficient, and for PCI bus, for example. But as time proved and technology advanced, it was clear that components required for embedded applications could not emanate from the PC ecosystem, and parts were developed specifically to address the unique requirements of embedded designs.

Today, the embedded marketplace has developed its own solutions with the suppliers and supply timelines that match embedded designers’ needs. The RapidIO ecosystem comprises market-leading component manufacturers and OEMs that have created a plethora of RapidIO products, all of which deliver the highest performance at the best total cost of ownership.

At the time this article was written, four high-performance switch vendors joined with two DSP and processor vendors to form a base for six FPGA and ASIC suppliers, a dozen IP providers, and more than 20 board suppliers to the VME and AdvancedTCA markets. Software for operating systems and network management complement the total solutions available using RapidIO technology.

Too many RapidIO-based products are shipping to list them all here, however the 80-plus products and nearly 50 profiles of our members can be found in the RapidIO Product Showcase at www.RapidIO.org/productshowcase.

Interoperability

Interoperability is an important issue to OEM design engineers. Recognizing that, the RapidIO Trade Association took a unique approach in developing the RapidIO standard, starting at the root of design to address interoperability. The RapidIO Trade Association, unlike other groups, has a standard bus functional model for semiconductor and system design simulation. Before vendors tape out or, in many cases before they build their first system, they are ensured that the semiconductor or systems investment they made will interoperate with other vendors. Freescale Semiconductor developed a bus functional model for RapidIO and donated it to the trade association. A RapidIO working group manages this full-function model, and trade association members fund its maintenance in an open source model. This value-add is available openly to all members of the organization and has proven to be both popular and effective.

In addition to addressing interoperability at the design stage, the RapidIO Trade Association has developed a set of checklists to ensure components can be thoroughly tested for compliance to the specification. The interoperability is guaranteed by creating a gold standard checklist for lab testing. Evidence of this success was seen at a recent Global Design Summit hosted by the RapidIO Trade Association where components from 16 vendors were demonstrated, successfully working together.

The RapidIO community has worked together like no other standards organization to test and put in place the capability
to test the elements of the RapidIO ecosystem. In 2005, Tundra Semiconductor kicked off an effort to facilitate an interoperability lab, RIOLAB. RIOLAB commenced full operations and started accepting reservations for test sessions from vendors and OEMs involved in RapidIO-based product development in July of this year. The vision is for this lab to develop into an independent testing facility to be used by all vendors to test device interoperability and run the checklist. The goal of the lab is to provide a level of testing OEMs can rely on for specification compliance assurance so they can focus their efforts on systems development. This is just one example of the unique collaboration found in the RapidIO community.

**Interworking**

With an ever-present push to lower engineering and system costs, leveraging industry standards has greatly increased in importance. To limit the software impact, the RapidIO standard retained many of the usage paradigms previously supported in bus-based protocols such as address-based reads and writes, messaging, and doorbell interrupts. These paradigms are the base upon which RapidIO works with other interconnects. By adopting a clear-cut destination-based transport model, RapidIO reduced switch gate count and die size by minimizing the header fields that must change as packets pass through a switch. This results in reduced implementation cost and lower overall complexity. With most of the protocol implemented in hardware, software drivers are far simpler than a typical Ethernet TCP/IP stack and can depend on the existence of standardized services.

The RapidIO specification is a single uniform protocol with limited options and consistent protocol layering; PCI is easily translated using RapidIO Load/Store operations, which by design are matched one to one with PCI bus and PCI Express operations. RapidIO adds value by its hierarchical nature and was designed from the beginning to provide robust and reliable data delivery. To handle Ethernet packets, RapidIO has developed an encapsulation protocol to take advantage of the efficiency and low, consistent latency when transporting Ethernet over RapidIO. A significant performance improvement can be made to the delivery of Ethernet across the fabric using RapidIO. Members of the RapidIO software working groups are working on standard usage models for solidifying the complementary roles of PCI Express, RapidIO, and Ethernet in next-generation systems.

**Technology road map**

The RapidIO Trade Association technical working groups are supporting current RapidIO technology deployment with a road map to higher performance and greater functionality. The current 1.3 version of the specification pulls together all of the advanced multicast and data streaming enhancements that have been approved. Current specification additions fall into two major areas of concentration: new higher-performance physical layer and significant data plane enhancements.

New higher-performance physical layers have been developed to support growing demands for 5 Gbps and 6.25 Gbps channel rates. These new speeds will use currently available PHY technology in a partnership with the Optical Internetworking Forum (OIF). These features include:

- **Rev 2.0 backwards compatibility**
- **Link width options of 1x, 2x, 4x, 8x, and 16x**
- **Signaling rates of 1.25, 2.5, 3.125, 5.0, and 6.25 Gbps**
- **Hot-plug support at the electrical level**

Data plane enhancements offer carrier grade data fabric performance driven by the needs of our OEM members. The goal of these features is to take advantage of backplane applications that have high demands for efficiency and robust data delivery. The RapidIO Trade Association is developing a new Data Streaming Packet Format with the addition of Virtual Channels (VCs) to the serial physical layer, new Endpoint Flow Control Arbitration, new Traffic Management Spec, and Virtual Output Queue (VoQ). These additional enhancements to the specification are currently under member ballot review and are expected to be released at the end of 2006.

RapidIO has found its way into hundreds of systems and labs around the world. RapidIO base architecture’s design activity and systems deployment have exploded in the past year. The availability of a broad base of semiconductors, boards for VME and AdvancedTCA, and software combined with exciting new applications like triple play, storage, signal processing, and video have made RapidIO the number one choice of designers in the embedded market.

**RapidIO – A solid, open technology**

RapidIO is a strong and evolving specification – a world-class ecosystem of embedded suppliers, interworking capabilities with other interconnects and tested interoperability. The RapidIO Trade Association is proud of the fact that RapidIO is and will continue to be driven by the embedded industry, for the embedded industry. We are open for business with products shipping to OEMs who wish to test, evaluate, and design their next several generations of equipment. RapidIO is, above all, an open standard: open for participation and input from vendors and OEMs and open technology in the truest sense of the words.

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Core of next-generation base station architectures utilize Serial RapidIO switches to interconnect multiple DSPs

By Bill Beane and Manish N. Patel

Serial RapidIO’s highly tuned support for DSP clusters allows equipment designers to develop very flexible and scalable architectures in a cost-efficient manner. With Serial RapidIO, for example, a base station designer can build a DSP-intensive system for macro cell applications. This allows the rapid deployment of new technology to support wide areas of coverage and reuse of the original design in scaled-down solutions for micro- or pico-based environments that deliver the desired density level without undue cost.

Figure 1 depicts the DSP-centric architecture of a potential baseband card in a system that’s trying to support a combination of technologies, such as UMTS and CDMA2000. Such a card would likely support both transmit and receive operations. It would need to support a wide range of mathematical operations or algorithms to include channelizing, spreading, and modulation in the transmit side and rake receiving, channel estimation, and coherent detection on the receive side. Typically, such a baseband card has a cluster of DSPs supported by hardware accelerator blocks that provide additional Chip-Rate Processing (CRP) support, whether as standard solutions or in the form of FPGAs or ASICs. The number of DSPs utilized depends upon the processing requirements of the baseband card. A Serial RapidIO-enabled DSP can perform various WCDMA functions, including chip rate and symbol rate processing. As the numbers of users or antenna streams are increased, additional DSPs can easily be added over the RapidIO interface to provide load balance.

A Serial RapidIO-based switch architecture is highly flexible and scalable. It provides designers a wide range of flexibility in assigning the functional partitioning of key application tasks among the various processing endpoints. Traffic and processing power can also be shifted from one device to another at runtime since the architecture is not tightly coupled with algorithms anymore. The architecture readily supports scalability as well, facilitating the process of increasing or reducing the number of endpoints as needed to accommodate specific application performance and cost requirements. For example, the number of CRPs and DSPs can be changed easily to adapt the same design for pico to macro base stations.

All of the components needed to implement such an optimized baseband solution are now readily available in the Serial RapidIO ecosystem, along with appropriate test/analyzer and software solutions to permit efficient system development. Such critical devices as microprocessors and DSPs are available from major industry icons such as Freescale Semiconductor and Texas Instruments, and Altera and Xilinx support the FPGA solutions. The necessary switch fabric solutions are also available from a number of vendors, including IDT, PMC-Sierra, and Tundra Semiconductor.

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Embedded systems: the future of RapidIO technology

By Ernie Bergstrom

In fall 2003, Crystal Cube Consulting (CCC) projected in a report on bus wars that Advanced Switching Interconnect (ASI) would not be able to roll out their ASI high-speed bus architecture until early 2006 and that by then RapidIO would have a commanding lead. Well, we have seen not only that come to pass, but also recently Intel and the ASI-SIG plan for a rollout has been postponed for the foreseeable future. This recent development is, of course, very good news for the RapidIO Trade Association and for RapidIO’s future support of embedded system applications.

Being able to decide on an ideal communication fabric for connecting various components within a system is a very critical decision system designers must make. Not unlike the telecommunications industry has done for years using proprietary solutions, much effort was invested in research and development of in-house communication fabrics that used proprietary communication protocols. The fabrics in question were always cost prohibitive and used bridging devices that would convert standard protocols to those supported by the fabric, adding to the overall cost of building the system.

At the other end of the spectrum, standard interconnect technologies have been continually adding salient features. A great deal of this kind of activity can be tied directly to market pressures to deliver scalable, reliable, and high-performance interconnects that can support applications such as IPTV and VoIP. Consequently, and out of necessity, companies are now slowly moving toward adopting standard technologies as their system interconnects of choice. RapidIO is one such emerging standard that provides high-performance interconnect for chip-to-chip, board-to-board, and chassis-to-chassis communications.

Developed as an open standard, RapidIO is designed to address the needs of present and future high-performance embedded systems. In embedded system applications, RapidIO has limited to no impact on the software infrastructure that operates over it. It can be implemented with relatively few transistors, and offers low operation latency and high bandwidths. High-performance embedded equipment often contains a separate control plane and data-forwarding plane. The data-forwarding plane is responsible for moving data through the system while the control plane manages the data movement. RapidIO provides all of the necessary attributes to be useful in the control plane. RapidIO, in some applications, may also be useful as the basis for data-forwarding plane implementations.

High-performance embedded systems are typically composed of DSP farms, collection-integrated processors, ASICs, and FPGAs tightly coupled together. These integrated processors are often quite specialized for each task. For example, network processors are specially designed to process packets. Communications processors are designed to convert communications streams from one protocol to another (for example, from Ethernet to ATM). DSPs perform tasks such as voice compression/decompression and echo cancellation.

Embedded systems require low latency across the switch fabric and endpoint components; they require neither the cache coherency capability nor PCI software transparency. RapidIO is well suited for high-performance embedded applications within embedded systems. All major DSP vendors have committed to RapidIO as the interconnect technology in their embedded systems. While this doesn’t exclude their consideration for advanced switching, which has been delayed indefinitely, we believe RapidIO has a strong lead and that the momentum will result in capturing higher market share in embedded systems applications.

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