RapidIO technology is destined to become one of the dominant embedded interface technologies in a wide range of applications, most notably serving as the primary interconnect for high-speed embedded backplanes and system-level fabrics. According to a report from Crystal Cube Consulting[1], RapidIO technology will experience a five-year average Compounded Annual Growth Rate (CAGR) of 39 percent in the DSP market alone, with projected shipments of almost 78.5 million ports in 2011, as shown in Figure 1.

Several factors are responsible for the continued and rapidly progressing success of RapidIO technology in the market. These include the increased need for high-speed serial interfaces across markets and applications, the technical superiority of RapidIO links over Ethernet in embedded high-speed backplane applications and as a system-level fabric, the aggressive penetration of RapidIO interfaces integrated onto DSPs, the demise of the Advanced Switching Interconnect (ASI), and the maturity of the RapidIO ecosystem to carry the market in the long term.

![Figure 1](image)
The need for high-speed serial interconnects

Increases in system performance necessitate innovations in interfaces that support higher bandwidth while enabling greater port density and reduced power consumption. Inherent limitations in parallel bus architectures cannot meet these needs and are the foundation of many system performance bottlenecks. For example, signal skew makes it impractical to further increase bus speeds while widening buses increases design complexity and cost because of the need for higher pin counts, more PCB layers, and a general encroachment on scarce board space.

For these reasons, the market is turning to high-speed serial interfaces such as RapidIO technology, 1 Gbps and 10 Gbps Ethernet, PCIe, and InfiniBand. Each of these technologies has particular strengths and applications in which it generally provides the best-performing and most cost-effective approach. PCIe, for example, owns the PC desktop market while InfiniBand has been repositioned as a storage area network and clustering technology.

Ethernet, while the leading interface technology in the LAN, must stretch beyond reasonable limits to extend its already broad reach into high-speed backplane and system-level fabric applications. Ethernet was designed for large-scale networks where each node could be expected to have its own powerful processing resources. As a consequence, Ethernet requires a large, flexible software stack that pushes many key functions such as guaranteed delivery and messaging to higher protocol levels. This increases overall latency, compromises reliability, and makes it inefficient (maximum utilization is about 25-35 percent in 10 Gbps links) to use in applications passing control plane traffic.

Performance can be improved with hardware-based offload engines, but these are effectively proprietary implementations, making them complex to design with and difficult to maintain while negatively affecting system interoperability. Additionally, Ethernet’s often-touted economies of scale advantage doesn’t apply to backplane and fabric applications that require specialized functionality. This significantly limits the number of Ethernet-based products and vendors supporting these applications.

The RapidIO specification, for its part, was specifically designed as a next-generation front-side bus that could also serve as an efficient system-level interconnect in ways that a software-based protocol like Ethernet cannot. Designed specifically for embedded in-the-box and chassis control plane applications, RapidIO provides minimal latency, limited software impact, and protocol extensibility while simplifying switch architectures and achieving data rates from 667 Mbps to 30 Gbps.

With efficient headers, hardware-based protocol processing, and key functions integrated into the base protocol – including guaranteed delivery, read/write operations, messaging, data streaming, quality of service, data plane extensions, and protocol encapsulation, all without the overhead of higher-layer protocols – RapidIO interconnects achieve 2.5 times more effective bandwidth per link than GbE at an equivalent cost. Furthermore, Serial RapidIO links can reliably consolidate both data and control planes onto a single, robust fabric, substantially simplifying system design while minimizing cost by reducing the number of interconnect technologies and ports a system must support.

Aggressive market growth

One way to measure the market success of RapidIO technology in embedded backplane and system-level fabrics is to evaluate its penetration into the DSP market. DSPs are the core of many applications such as wireless communications, which represented 64 percent of the overall DSP market at the end of 2006 (see Figure 2), and therefore require a serial interconnect technology integrated directly onto the processor to achieve the greatest efficiencies when passing large amounts of data. Tracking the number of DSPs sold in particular applications makes it possible to estimate Serial RapidIO technology’s overall adoption rate.

While PCIe had initial success in the DSP market, in the past two years, the PCIe industry moved away from PCIe to Serial RapidIO interconnect technology. This shift arose from the recognition of PCIe’s inappropriate fit for embedded backplane applications and its subsequent focus on the PC desktop market. PCIe supporters responded by developing the ASI, which was specifically designed to resolve PCIe’s generally acknowledged shortcomings in fabric architectures and replace PCIe slots in the backplane market.

However, ASI did not experience the success its creators had hoped for. As Ernie Bergstrom, VP and chief analyst at Crystal Cube Consulting, states in his report, “Since the ASI architecture is essentially dead, the remaining viable architectures for high-speed backplanes are principally RapidIO technology and Ethernet.”

These changes in market direction help account for the success of Serial RapidIO-based DSPs in capturing approximately 20 percent of the overall DSP market in 2006. As DSP vendors continue to introduce Serial RapidIO interfaces to more of their devices, market share is expected to increase from $1.5 billion of the overall $7.5 billion DSP market in 2006 to more than $4.71 billion of the overall $13.7 billion market in 2011, representing integration into more than 34 percent of DSPs worldwide (see Figure 3).

In addition, Serial RapidIO technology has widespread industry support dedicated to meeting the needs of developers in both the short and long terms. Serial RapidIO technology has an extensive ecosystem driven by such industry leaders as AMCC,
Freescale, and Texas Instruments, and for embedded backplane and system-level fabric applications, Serial RapidIO technology offers more product options and economies of scale than Ethernet. According to Bergstrom’s report, “Technologies like the RapidIO standard have developed a sufficient ecosystem to warrant careful evaluation alongside Ethernet.”

On course to greater adoption
RapidIO was designed from the start to be the most efficient interface for high-speed applications capable of meeting the throughput needs of data-intensive applications while providing the reliability required for control plane data transfers. With hardware-based protocol processing and a rich feature set defined within the base specification, Serial RapidIO stabilizes implementations, guaranteeing consistency and interoperability across the industry while leading to more choices for developers.

With strong industry support and a firm market base, RapidIO technology is well-established on its course to becoming the principal interconnect of embedded backplane and system-level fabric applications. ECD

Tom Cox is executive director of the RapidIO Trade Association, where he is responsible for the association’s future direction. Most recently, he was director of strategy at Tundra Semiconductor. Prior to that, he spent five years with IBM Microelectronics and was responsible for the PCI product line. Tom has held executive and engineering positions with ATI Technologies Inc., LSI Logic Corporation of Canada, Inc., Litton Systems Canada, and Philips Electronics Canada. He is a founding member of the PCI-SIG and has served in industry workgroups within PICMG, VITA, and NPF. Tom pursued advanced training in mathematics and electrical and computer engineering through the University of Southern California (USC), Humber College in Rexdale, and Mohawk College in Hamilton.

RapidIO Trade Association
512-305-0070
tom.cox@rapidio.org
www.rapidio.org

<table>
<thead>
<tr>
<th>Worldwide DSP revenues vs Serial RapidIO</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>CAGR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total DSPs ($B)</td>
<td>$7.5</td>
<td>$8.4</td>
<td>$9.5</td>
<td>$10.8</td>
<td>$12.5</td>
<td>$13.7</td>
<td>12.8%</td>
</tr>
<tr>
<td>% Change</td>
<td>12.0%</td>
<td>13.1%</td>
<td>13.7%</td>
<td>15.7%</td>
<td>9.6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial RapidIO DSPs ($B)</td>
<td>$1.50</td>
<td>$1.74</td>
<td>$2.20</td>
<td>$2.80</td>
<td>$3.76</td>
<td>$4.71</td>
<td>25.7%</td>
</tr>
<tr>
<td>% Change</td>
<td>16.0%</td>
<td>26.4%</td>
<td>27.3%</td>
<td>34.3%</td>
<td>25.3%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>% Serial RapidIO DSPs to total DSPs</td>
<td>20.71%</td>
<td>23.16%</td>
<td>25.93%</td>
<td>30.03%</td>
<td>34.38%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 3

References

(All figures courtesy of Crystal Cube Consulting.)