The RapidIO Trade Association recently released a set of extensions to the base RapidIO protocol. These extensions, which have been in development for 18 months, will be able to control congestion that sometimes occurs in high-utilization data plane applications. These extensions complement the link-based flow control mechanisms already included in the RapidIO architecture and support the development of larger and more complex RapidIO-based systems, such as media gateways, radio network controllers, and routers used in mobile networks.

Work on the flow control extensions began in early 2002 at the instigation of major system OEMs that were interested in deploying the RapidIO interconnect as a system-wide combined control and data plane interconnect. They were concerned that, in complex systems, sole reliance on the link-based flow control mechanism might expose the system to issues such as second-order, head-of-line blocking that, in the worst case, could lead to performance collapse.

A task group performed extensive simulation work with queue-based system models of the RapidIO interconnect. Using expected traffic patterns, the group evaluated various proposed flow control solutions. After review of the simulation results and the impact of the proposed changes to existing RapidIO devices and infrastructure, the group settled on a relatively simple directed XON/XOFF mechanism as the preferred solution.

The task group found this mechanism to keep mean packet delay much closer to an ideal system with infinite buffers than link-flow control alone. For example, simulation models showed that as network utilization increased from 70 percent to 90 percent, the mean packet delay increased by only 22 percent over the ideal versus 89 percent when they used link-flow control alone.

The extensions, which introduce a new logical layer transaction type called Congestion Control Packets (CCP), are transparent to existing RapidIO switch devices, and designers can easily implement them within RapidIO end points. The RapidIO architecture design easily supports enhancements such as these flow control extensions.

The RapidIO Trade Association also recently announced the integration of the Advanced Fabric Interface working group into the Trade Association, and formed a RapidIO task group to create the data streaming specification for data plane applications. The primary responsibility of this group is to define standard transaction formats for the transport of typical data plane transaction payloads across interoperable RapidIO fabrics. Example payload types would include ATM cells, Ethernet packets, and SONET frames.

While RapidIO devices already can provide transport of these data types either as messages or as memory-to-memory transfers, the additional specification work provides a standardized approach. The purpose of this approach is to aid in the development of broadly interoperable RapidIO-based semiconductor devices and subsystems.

The diagram to the right in Figure 1 shows how the flow control extensions and the data plane extensions enable the RapidIO interconnect architecture to solve virtually all interconnect needs within embedded computing systems.

While it is true that the operational characteristics of control planes and data planes are different, it is quite feasible to develop an interconnect framework that supports both applications well. RapidIO accomplishes this task by providing a partitioned specification hierarchy of physical, transport, and logical transaction layers.

The RapidIO Physical Layer offers a reliable flow-control managed link technology based on established differential driver technology, which such organizations as IEEE and OIF standardize.

The RapidIO Transport Layer offers a simple and elegant system-mapping model, which supports the single-system connectivity of hundreds to thousands of devices.
Several Logical Transaction Layers are available that provide support for PCI-like I/O transactions, Ethernet-like messages, transactions to support coherency between cache-equipped microprocessors distributed through a system and, now in development, support for encapsulated transport of streaming data types like Ethernet and ATM.

An advantage of the RapidIO architecture is its optimization of low-bit overhead versus robust functionality. Other approaches have much higher transaction overhead either in bits, on the wire, or in software. These result in lower effective utilization. Another advantage is the ability to encompass control and data path applications under one specification hierarchy. This reduces the overall investment in maintaining multiple types of interconnects within a system domain.

The widespread use of the open standard RapidIO technology within embedded computing systems will greatly simplify the system development task. A common set of wires and protocols throughout the system will allow for the virtualization of I/O and will allow companies to not waste resources developing ASICs or FPGAs to bridge a variety of incompatible buses but rather to focus their resources on their own unique value propositions.

Contact the RapidIO Trade Association directly for more information.

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